APPENDIX A

Please amend claims 95-97 as follows.

--95. (Amended) An image processing system comprising:

a read only memory storing [an] digital image information;

[an] a memory accessing circuit coupled to the read only memory and accessing the digital image information from the read only memory; [and]

[a display] an image processor coupled to the memory accessing circuit and generating a rotated and translated image by rotation and translation processing of the digital image information accessed by the memory accessing circuit; and

a projection display medium coupled to the image processor and displaying an image in response to the rotated and translated image generated by the image processor.

--96. (Amended) An image processing system comprising:

a database read only memory storing a database image;

an image read only memory storing a portion of the database image;

an image read only memory loading circuit coupled to the database read only memory and coupled to the image read only memory and loading a portion of the database image stored by the database read only memory into the image read only memory; [and]

an image processor coupled to the image read only memory and generating [a] processed digital image information by processing the digital image information stored in the image read only memory; and

a three dimensional display medium coupled to the image processor and displaying an image in response to the processed digital image information generated by the image processor.

--97. (Amended) A display system comprising:

a read only memory storing [an] digital image information;

[a display] an image processor coupled to the read only memory and scanning out the digital image information stored in the read only memory; and

a display medium coupled to the [display] image processor and displaying the digital image information scanned out by the [display] image processor.

Please add claims 339 - 341 as follows.

--339. An image processing system comprising:

a memory storing an image;

an accessing circuit coupled to the memory and accessing the image from the memory;

a first memory coupled to the accessing circuit and storing prior pixel image information in response to the image accessed by the accessing circuit, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a spatial interpolation circuit coupled to the first memory and coupled to the second memory, the spatial interpolation circuit generating spatially interpolated image

information in response to the prior image information stored in the first memory and in response to the next image information stored in the second memory;

a first integer circuit coupled to the spatial interpolation circuit and generating spatially interpolated integer image information by rounding the spatially interpolated image information generated by the spatial interpolation circuit;

a temporal interpolation circuit coupled to the first integer circuit and generating temporally interpolated image information in response to the spatially interpolated integer image information generated by the first integer circuit;

a transform processor coupled to the temporal interpolation circuit and generating transformed image information in response to temporally interpolated image information generated by the temporal interpolation circuit;

a weight circuit generating weight information;

a scale factor circuit generating scale factor information;

a scaling and weighting circuit coupled to the scale factor circuit, coupled to the weight circuit, and coupled to the transform processor, the scaling and weighting circuit generating scaled weighted image information in response to the transformed image information generated by the transform processor, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit;

a second integer circuit coupled to the scaling and weighting circuit and generating scaled weighted integer image information by rounding the scaled weighted image information generated by the scaling and weighting circuit; and

a display processor coupled to the accessing circuit and coupled to the second integer circuit, the display processor generating a rotated and translated image by rotation and translation processing of the image accessed by the accessing circuit in response to the scaled weighted integer image information generated by the second integer circuit.

--340. An image processing system comprising:

a database memory storing a database image;

an image memory storing a portion of the database image;

an image memory loading circuit coupled to the database memory and coupled to the image memory and loading a portion of the database image stored by the database memory into the image memory;

an image processor coupled to the image memory and generating a processed image by processing the image stored in the image memory.

a first memory coupled to the image processor and storing prior pixel image information in response to the image processed by the image processor, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a spatial interpolation circuit coupled to the first memory and coupled to the second memory, the spatial interpolation circuit generating spatially interpolated image information in response to the prior image information stored in the first memory and in response to the next image information stored in the second memory;

a first integer circuit coupled to the spatial interpolation circuit and generating spatially interpolated integer image information by rounding the spatially interpolated image information generated by the spatial interpolation circuit;

a temporal interpolation circuit coupled to the first integer circuit and generating temporally interpolated image information in response to the spatially interpolated integer image information generated by the first integer circuit;

a transform processor coupled to the temporal interpolation circuit and generating transformed image information in response to temporally interpolated image information generated by the temporal interpolation circuit;

a weight circuit generating weight information;

a scale factor circuit generating scale factor information;

a scaling and weighting circuit coupled to the scale factor circuit, coupled to the weight circuit, and coupled to the transform processor, the scaling and weighting circuit generating scaled weighted image information in response to the transformed image information generated by the transform processor, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit; and

a second integer circuit coupled to the scaling and weighting circuit and generating scaled weighted integer image information by rounding the scaled weighted image information generated by the scaling and weighting circuit.

--341. A display system comprising:

a memory storing an image;

a display processor coupled to the memory and scanning out the image stored in the memory;

a first memory coupled to the display processor and storing prior pixel image information in response to the image scanned out by the display processor, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a spatial interpolation circuit coupled to the first memory and coupled to the second memory, the spatial interpolation circuit generating spatially interpolated image information in response to the prior image information stored in the first memory and in response to the next image information stored in the second memory;

a first integer circuit coupled to the spatial interpolation circuit and generating spatially interpolated integer image information by rounding the spatially interpolated image information generated by the spatial interpolation circuit;

a temporal interpolation circuit coupled to the first integer circuit and generating temporally interpolated image information in response to the spatially interpolated integer image information generated by the first integer circuit;

a transform processor coupled to the temporal interpolation circuit and generating transformed image information in response to temporally interpolated image information generated by the temporal interpolation circuit;

a weight circuit generating weight information;

a scale factor circuit generating scale factor information;

a scaling and weighting circuit coupled to the scale factor circuit, coupled to the weight circuit, and coupled to the transform processor, the scaling and weighting circuit generating scaled weighted image information in response to the transformed image information generated by the transform processor, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit;

a second integer circuit coupled to the scaling and weighting circuit and generating scaled weighted integer image information by rounding the scaled weighted image information generated by the scaling and weighting circuit; and

a display medium coupled to the display processor and coupled to the second integer circuit, the display medium displaying the image scanned out by the display processor in response to the scaled weighted integer image information generated by the second integer circuit.